Compact Model of Dielectric Charging in RF MEMS Capacitive Switches
Prasad Sumant, Andreas C. Cangellaris, Narayan R. Aluru

Overview

RF MEMS capacitive switches show great potential for use in wireless communication device. However, their widespread insertion in commercial products requires further improvements in their long-term reliability. Dielectric charging is one of the factors that impact switch reliability. Dielectric charging is understood to mean the accumulation of electric charge in the insulating dielectric layer between the two electrodes of the capacitive RF MEMS switch. It can cause the switch to either remain stuck after removal of the actuation voltage or to fail to contact under application of pull-in voltage. Considerable effort has been devoted to both the experimental characterization of dielectric charging and the development of models that can be used to predict the impact of dielectric charging on electro-mechanical behavior of a capacitive switch. This investigation has led to useful quantitative information that can be used for predictive assessment of performance degradation of an RF MEMS capacitive switch during operation. Such capability serves as a computer-aided accelerated testing of the switch.

For such capability to become readily available to designers, the pertinent computer model must be cast in a form that is seamlessly compatible with MEMS CAD tools such as Coventor’s Architect [1]. Over the past year work in our group focused on the development of such a model for the quantitative description of dielectric charging with the following attributes:

- It constitutes a generalization of the one-dimensional models reported in the literature to date;
- Utilizes experimentally-obtained data to extract parameters used for the description of the electrical properties of the model;
- Enables the calculation and monitoring of the temporal evolution of charge accumulation at the top and bottom surfaces of the insulating dielectric film;
- Enables simulation of repeated on–off operation of the switch for switch life time and reliability studies;
- Provides a means for the incorporation of the impact of the surface roughness of the electrode-dielectric interface on charge accumulation.

The proposed model relies upon the physical interpretation of the electro-quasi-static physics governing the buildup and evolution of dielectric charging in terms of a multi-layer capacitor model, where variation in material conductivity and permittivity in the layers result in charge buildup between the layers. The model has been described in the literature and will not be repeated here [2]-[3]. In this short description we limit ourselves to the demonstration of the ability of the model to correctly reproduce experimentally-observed dielectric charging and its use for the expedient computer-aided investigation of how the choice of different control voltage waveforms impact the buildup of charge in an RF MEMS switch.

Discussion

Illustrated in Fig. 1 on the left is the one-dimensional (1D) compact model used for system level modeling of such MEMS switches. It highlights the kind of model that will be needed for dielectric charging. This model represents an ideal switch. However, processing conditions result in inhomogeneities and imperfections in both the electrodes and the insulating dielectric. For example, due to surface roughness the interface between the metal and the dielectric is not perfectly planar. Macroscopically, this can be viewed as a spatial variation in the electrical properties of the dielectric, namely, its electric permittivity and its conductivity. As is well known, surfaces of discontinuity of the material electrical parameters become regions of accumulation of charge. In a similar manner, defects within the volume of the dielectric material itself and, more generally, the presence of variations in its macroscopic electric properties, lead to accumulation of charge throughout the bulk of the dielectric. For modeling simplicity and in the con-
text of 1D modeling, we use a single sheet of charge, located at a certain distance, \( b \), from the bottom electrode to account for this bulk charge in the model. Based on the discussion above, for charge to accumulate at this plane the electrical properties of the dielectric must exhibit a discontinuity across the plane.

Let \( V(t) \) be the impressed voltage between the two electrodes (right side of Fig. 1). The one-dimensional nature of the proposed model and its piece-wise homogeneous material properties imply that the electric field is uniform in each layer. Let \( \rho_{ab} \) represent the surface charge density at the interface. It is, then,

\[
\rho_{ab} = (\varepsilon_a E_a - \varepsilon_b E_b)
\]

where \( \varepsilon_i, \ i = a, b \), are the electric permittivities of the two layers. Application of charge conservation at the dielectric interfaces yields

\[
(\sigma_a E_a - \sigma_b E_b) + \frac{\partial}{\partial t}(\varepsilon_a E_a - \varepsilon_b E_b) = 0
\]

where \( \sigma_i, \ i = a, b \) are the conductivities of the two layers. Finally, the equation

\[
aE_a + bE_b = V(t)
\]

closes the system for the determination of the temporal evolution of \( E_a(t), E_b(t) \). More specifically, given \( V(t) \) the system of (1)-(3) can be solved for the calculation of the electric fields in the three layers, which, in turn, through (1),(2), can be used to obtain the temporal variation of the charge accumulation. The above equations can be simplified to arrive at a charging equation of the form,

\[
\frac{\partial \rho_{ab}}{\partial t} + B \rho_{ab} = A
\]

where \( A \) and \( B \) are given by,

\[
A = \frac{\sigma_b \varepsilon_a - \sigma_a \varepsilon_b}{b \varepsilon_a + a \varepsilon_b} V, \quad B = \frac{b \sigma_a + a \sigma_b}{b \varepsilon_a + a \varepsilon_b}
\]

Finally, using well-known results, the shift in actuation voltage due to charge accumulation is given by,

\[
\Delta V = \frac{b \rho_{ab}}{\varepsilon_b}
\]

The model parameters (layer permittivities and conductivities) are defined by making use of the experimental characterization of the bulk dielectric charging process as documented in [3]. More specifically, we make use of measured data of dielectric charge density accumulation, \( Q(t) \), obtained from transient current measurements [9]. A plot of \( Q(t) \) for different voltages reported in [3] is shown in Fig. 2 (blue line with ‘o’). The following strategy is used for obtaining the conductivities of the two layers.

- Pick a curve for the accumulated charge density \( Q(t) \) for a particular voltage.
- Calculate model parameters \( A \) and \( B \) (eq. (4)) through a non-linear least squares algorithm. \( A \) and \( B \), in turn, yield the conductivities through eqs. (5) and (6) as all other model parameters are already defined.
- Note that \( A \) is related to the steady state value while \( B \) is related to the time constant of the charge density accumulation. It has been experimentally observed that time constant does not vary with the applied voltage.
- Once \( B \) is found for one voltage, for other voltages only \( A \) needs to be determined. Thus, only steady-state values of charge/actuation voltage shift are needed for determining \( A \).

The above methodology was used to define the conductivities in the proposed model using the data in [3]. The model was then used to calculate charge accumulation and was compared to the experimentally obtained results. Fig. 2 depicts the comparison. Very good agreement is observed. For the simulated curves in Fig. 2, the values of \( A \) for 40 V, 35 V and 30 V obtained through the above mentioned process were
2.627e-5, 1.624e-5 and 1.005e-5 (A/m²) respectively and the value of $B$ was 0.026 s⁻¹. Plotted in Fig. 3 is the conductivity of layer ‘b’, illustrating its non-linear dependence on the voltage.

With all parameters defined, the model lends itself to the calculation of dielectric charge accumulation for any control voltage waveform. Bipolar control voltage waveforms have been proposed as a means to limit dielectric charging [3]. The proposed model provides for a computationally efficient way for evaluating dielectric charging under different control voltage waveforms and its impact on actuation voltage. Following [3], the change in actuation voltage versus time was computed using our model for three different control waveforms with attributes given in [3]. As depicted in Fig. 3, the predictions from our model (solid lines in the graph) are in excellent agreement with the experimental values reported in [3]. Waveform 3 is seen to minimize the effect of dielectric charging.

The proposed model can be cast in the form of a SPICE circuit consisting of a capacitor, a variable resistor and a voltage controlled current source. This model is very efficient to simulate using a nonlinear, SPICE-like, circuit simulator. For example, the simulation for the prediction of dielectric charge accumulation after four million cycles requires 600 s of computation time on a PC with 1 GB RAM and 1.76 GHz Intel Pentium M processor.

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**References**


[4]

![Diagram](image)

**Figure 1.** Left: One-dimensional model showing the OFF and ON states of an ideal capacitive switch. Right: Proposed two-layer Maxwell capacitor model for the temporal evolution of dielectric charging in the switch.
Figure 2. Comparison of model prediction with experimentally obtained charge density.

Figure 3. Bipolar waveforms: comparison of model prediction with results from experiment [3].